SN – 668

13

I Semester B.C.A. Degree Examination, November/December 2017
(Repeaters) (Y2K8 Scheme)
BCA 104 – ELECTRONICS

Time : 3 Hours Max. Marks : 60/70

Instructions : *1)* ***60*** *marks is only for those who admitted prior to* ***2011 – 12.***
2) Section – ***D*** *is for those admitted from* ***2011 – 12*** *and Onwards.*

SECTION – A

I. Answer **any ten** questions. **(1×10=10)**

1) What is a semiconductor ?

2) Define the term electrical network.

3) State Kirchoff's Voltage Law.

4) Define short circuit.

5) Define Ripple factor of rectifier.

6) Define energy band.

7) Write the 2's complement of $10011101_{(2)}$.

8) Write the excess-3 code for $7_{(10)}$.

9) Define racing condition in JK flipflop.

10) Convert $11101_{(2)}$ into Graycode.

11) What is timing diagram ?

12) What is sequential logic circuit ?

P.T.O.

SECTION – B

II. Answer **any 5** questions. **(3×5=15)**

13) State and explain superposition theorem. **3**

14) Explain the operation of P-N junction diode with a neat diagram. **3**

15) Explain the terms knee voltage, forward bulk resistance and reverse resistance. **3**

16) Differentiate between Half-wave and Full-wave rectifier. **3**

17) Explain BCD code. **3**

18) Explain cell adjacency in K-map. **3**

19) What is delay flipflop ? Explain briefly. **3**

20) Explain decimal to BCD encoder with a neat diagram. **3**

SECTION – C

III. Answer **any 5** questions. **(7×5=35)**

21) a) Explain maximum power transfer theorem. **3**

b) Derive the relationship between time period and frequency. **4**

22) a) Explain the classification of semiconductors. **3**

b) Derive an expression for RMS value of an alternating current. **4**

23) a) Convert $1101.11010_{(2)} = (\ )_{10}?, (\ )_8$? **3**

b) Write a note on error detection and error correction codes. **4**

24) a) State and prove De-Morgan's theorem using truth table. **4**

b) Minimize the following standard SOP expression using Karnaugh map $\bar{A}BC + A\bar{B}C + A\bar{B}\bar{C}$. **3**

25) a) Construct AND and OR gates using NAND gate. Explain with truthtable. 4

b) Write a note on parity checkers and parity generators. 3

26) Explain full adder and subtractor circuit with a neat diagram and truthtable. 7

27) a) Explain SR flipflop with a logic diagram. 4

b) Differentiate between latch and flipflop. 3

28) a) Explain PIPO shift register with logic diagram and timing diagram. 4

b) Write a note on application of shift registers. 3

SECTION – D

IV. Answer **any one full** question. **(10×1=10)**

29) a) Explain half-wave rectifier with a neat diagram. 5

b) Write a note on IC families. 5

30) a) Explain Master-Slave flipflop with a neat logic diagram. 5

b) P.T. $(X + Y)(X + Z) = X + YZ$. 5
