



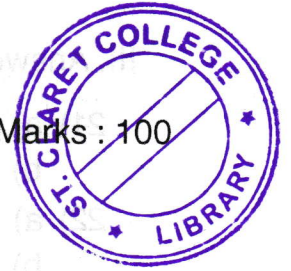
SN – 664

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V Semester B.C.A. Degree Examination, Nov./Dec. 2017
(CBCS) (F + R) (2016-17 and Onwards)
BCA 503 : COMPUTER ARCHITECTURE

Time : 3 Hours

Max. Marks : 100



Instruction: Answer **all** Sections.

SECTION – A

I. Answer **any ten** questions. **Each** carries **two** marks. (10×2=20)

- 1) Write the symbol, logical expression and truth table of NAND gate.
- 2) Give the classification of integrated circuits.
- 3) Distinguish between RAM and ROM.
- 4) Define Multiplexer and Demultiplexer.
- 5) What are the types of binary codes ?
- 6) Subtract $24_{(10)}$ from $13_{(10)}$ using 2's complement method.
- 7) Define opcode and operand.
- 8) What is BUN instruction ?
- 9) What are the two types of computer architecture based on registers ?
- 10) What are the different types of interrupts ?
- 11) Define access time and transfer rate.
- 12) Define Baud rate.

SECTION – B

II. Answer **any five** questions. **Each** question carries **five** marks. (5×5=25)

- 13) Explain the steps involved in the design of the sequential circuits.
- 14) Explain synchronous binary counter with logic diagram.
- 15) Discuss on error detection and correction codes briefly.
- 16) Explain any five register reference instructions.
- 17) With a block diagram, explain how BSA instruction executes.
- 18) Explain the addressing modes.
- 19) Explain DMA controller with a block diagram.
- 20) Write a note on virtual memory.

P.T.O.



SECTION – C

III. Answer **any three** questions. Each question carries **fifteen** marks. (3×15=45)

- 21) a) Simplify $F(ABCD) = \sum m (1, 3, 7, 11, 15) + \sum d (0, 2, 5)$ using K-map. 7
 b) What is a half adder ? Design a half adder using only NAND gates. 8
- 22) a) Explain decoder expansion with neat diagram. 7
 b) Discuss the parity generator and parity checker. 8
- 23) a) Explain common bus organization of basic computer with neat diagram. 8
 b) Distinguish between FGI and FGO. 7
- 24) a) What is a sub-routine ? Explain CALL and RETURN instructions. 8
 b) Explain the arithmetic logic shift with a neat diagram. 7
- 25) a) Explain I/O interface unit with a neat diagram. 8
 b) Write a note on isolated vs memory mapped I/O. 7

SECTION – D

IV. Answer **any one** question. Question carries **ten** marks. (1×10=10)

- 26) a) Explain 4-bit shift register. 5
 b) Explain the working of J-K flip-flop. 5
- 27) a) Explain interrupt cycle with suitable example. 6
 b) List the applications of EEPROM. 4